Abstract of the Disclosure:

An integrated circuit has a synchronous circuit and an asynchronous circuit. A clock-controlled input register circuit and an output register circuit for storing data are each connected to the synchronous circuit and the asynchronous circuit. Data are transferred from the synchronous circuit into the input register circuit, from where they are transferred into the asynchronous circuit and processed in the asynchronous circuit. Processed data are transferred into the output register circuit. A sequence controller generates a respective control clock signal for the register circuits in a manner dependent on the data processing duration of the asynchronous circuit. This enables a high data throughput between the synchronous circuit and the asynchronous circuit independently of a clock frequency of the synchronous circuit.

MPW/kf